Certificate of Completion

This is to certify that ***Singani Sanjeev Kumar*** *successfully completed 23 total hours of* ***Verilog for an FPGA Engineer with Xilinx Vivado Design Suite*** *online course on April 27, 2021*

Kumar Khandagle

Kumar Khandagle, Instructor

&

Udemy

Certificate no: **UC-e5fc6382-c95b-41ef-819f-0ea9023c2436**
Certificate url: **ude.my/UC-e5fc6382-c95b-41ef-819f-0ea9023c2436**
Version 3

#BeAble