Certificate of Completion

This is to certify that ***Devanshi*** *successfully completed 12 total hours of* ***Verilog HDL: VLSI Hardware Design Comprehensive Masterclass*** *online course on Aug. 20, 2020*

Shepherd Tutorials

Shepherd Tutorials, Instructor

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Certificate no: **UC-d1ab1ec2-b4f4-4c89-9d85-f3f60ce821c5**
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#BeAble