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Certificate no: UC-b9bc935c-ddf6-47ae-a3c4-b6e85b10cec6

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Reference Number: 0004

CERTIFICATE OF COMPLETION

Verilog HDL: VLSI Hardware Design Comprehensive Masterclass

Instructors **Shepherd Tutorials**

Ajay kashyap

Date **Aug. 13, 2026**

Length **12.5 total hours**