

Certificate of Completion

*This is to certify that Arijit Sengupta successfully
completed 1 hour of SoC Design 3: Systemverilog
Features for RTL Coding online course on Sept.
19, 2018*

Systemverilog Academy

Systemverilog Academy, Instructor

&



Certificate no: UC-PUZVF8UY
Certificate url: ude.my/UC-PUZVF8UY

#BeAble