

Certificate of Completion

*This is to certify that Vedant Garg successfully
completed 2 hours of SystemVerilog Design-1:
Start Programming Your Own IC in HDL online
course on Aug. 31, 2018*

Ajith Jose

Ajith Jose, Instructor

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Certificate no: UC-J16IYBBO
Certificate url: ude.my/UC-J16IYBBO

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