Certificate of Completion

This is to certify that ***Andrew Ekladious*** *successfully completed 3.5 total hours of* ***FPGA Embedded Design, Part 1 - Verilog*** *online course on Aug. 31, 2020*

Eduardo Corpeño
Eduardo Corpeño, Instructor

Marissa Siliezar
Marissa Siliezar, Instructor

&

Udemy

Certificate no: **UC-90bfdedc-b474-44ea-babb-9ed589441365**
Certificate url: **ude.my/UC-90bfdedc-b474-44ea-babb-9ed589441365**

#BeAble