Certificate of Completion

This is to certify that ***Ramesh Ramanaiah*** *successfully completed 18.5 total hours of* ***VLSI Digital Design using Verilog and hardware: Handson_temp*** *online course on July 18, 2020*

Hassan Uddin Shaik

Hassan Uddin Shaik, Instructor

&

Udemy

Certificate no: **UC-7a857fac-4ecc-4433-ba85-6ebf8b85b215**
Certificate url: **ude.my/UC-7a857fac-4ecc-4433-ba85-6ebf8b85b215**

#BeAble