udemy

Certificate no: UC-4f3799ed-aa5f-4d48-a288-b9dc0b0de4d3
Certificate url: ude.my/UC-4f3799ed-aa5f-4d48-a288-b9dc0b0de4d3
Reference Number: 0004

CERTIFICATE OF COMPLETION

Verilog for an FPGA Engineer with Xilinx Vivado Design Suite

Instructors **Kumar Khandagle**

Manish Kumar

Date **4 Jan 2025**
Length **16.5 total hours**