Certificate of Completion

This is to certify that ***Ashutosh Kumar*** *successfully completed 21 total hours of* ***Verilog for an FPGA Engineer with Xilinx Vivado Design Suite*** *online course on Feb. 26, 2021*

Kumar K.

Kumar K., Instructor

&

Udemy

Certificate no: **UC-20765821-019b-48b7-9b54-5ba82be43081**
Certificate url: **ude.my/UC-20765821-019b-48b7-9b54-5ba82be43081**
Version 3

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